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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,872	08/01/2003	Joseph H. End III	TN302	4647

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EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	**PAPER NUMBER**
2188	

MAIL DATE	DELIVERY MODE
10/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/632,872	Applicant(s) END, JOSEPH H.	
	Examiner Mardochee Chery	Art Unit 2188	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 19 September 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: *7,19 and 20*.
   Claim(s) rejected: *1-6,8-18,21 and 22*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
10/05/07

Continuation of 11. does NOT place the application in condition for allowance because: 1. Applicants argue on page 10, paragraph 3 of the remarks that "Nyusten is allegedly directed to a memory controler that includes an arbiter connected to a memory device via a single processing path. Specifically, in Flg. 3, Nyusten teaches a single processing path 334 that the arbiter utilizes to send successive commands and addresses to memory device. All memory request are processed through path 334 successively . Accordingly, Nystuen does not disclose, teach, or suggest an arbiter that assigns memory requests to first and second processing paths, recited in claim 1".

Examiner respectfully disagrees and would like to point out that in contrast to applicants' assumption that Nystuen teaches "a single processing path", in Fig. 3 Nystuen discloses two processing paths, processing paths 332 and 334, that Arbiter 308 uses to send commands and addresses to memory device 302.

2. Applicants further argue on page 10, paragraph 4 of the remarks that Shiozaki allegedly is directed to a storage control system that includes two controllers that direct successive memory requests over a single processing path. Specifically, in Fig. 1, Shiozaki teaches a single processing path 14 that a storage control unit 2 utilizes to send successive memory requests to main storage 3. All memory request are requests are processed through path 14 successively. Accordingly, Shiozaki does not disclose, teach, or suggest an arbiter that assigns memory requests to first and second processing paths as set forth in claim 1".

Examiner strongly disagrees and would like to point out that applicants' arguments are mere speculation that "in Fig. 1, Shiozaki teaches a single processing path 14 that a storage control unit 2 utilizes to send successive memory requests to main storage 3" and that contrary to applicants' presumption, Shiozaki discloses "requesting a fetch or store access to a first address array controller 4a via a line 10a; if the data is found, the controller 4a issues a data fetch request via a line 11a; if the requested data is missing, controller 4a issues a fetch request via a line 13a; col. 3, lines 60 to col. 4, lines 10" where it is readily apparent that controller 4a uses two different lines, lines 11a and 13 a, when requesting data.

3. Applicants still argue on page 10 paragraph 5 of the remarks that Payson allegedly, in Fig. 4, teaches "arbiter 470 with an input and output parallel bus 430. A single request is parallelized and transmitted over parallel bus 430 from SERDES RX 282. SERDES RX 282 converts serial data into parallel data that is transmitted over a single parallel bus 430 to arbiter 470. Arbiter 470 then transmits its output over a single 430. Therefore, Payson teaches an arbiter with a single request port (input parallel bus 430) and a single processing path (output parallel 430). Accordingly, Payson does not disclose, teach, or suggest an arbiter that assigns memory requests to first and second processing paths".

Examiner strongly disagrees with such contention. First of all, Examiner would like to point that applicants have mischaracterized and misconstrued the teaching of Payson. In contrast to applicants' assumption, Fig. 4 of Payson clearly discloses multiple input and output paths associated with arbiter 470 where it is worth mentioning that in Figure 4, bus 430 includes a plurality of lines and the arbiter issues grants over bus 430 for transmission over links 260 and that the arbiter FLARB 460 issues configuration information to each of the CASE devices 452 over independent control lines 435 between the CASE and FLARB devices [col. 9, lines 47-63]. Payson further discloses that all arbitration...must also be performed across those serial links, which are thereafter transposed into parallel links 440; col. 10, lines 5-9.

4. Applicants argue on page 12 paragraph 2 of the remarks that Nystuen fails to discloses, teach, or suggest at least the step of "assigning a memory request to one of the at least one controllers from one of the identified plurality of memory requesters that have not had previous memory requests granted during the current arbitration cycle using fixed priority logic, recited in claim 17.

Examiner respectfully disagrees. Nystuen discloses "compare circuit 550 compares bank address stored in history register 512 and bank address presently received to determine whether either is to the same bank stored in register 512; and a each successive command is loaded, the corresponding bank address is loaded into the history register where the bank control circuit generates a bank precharge command if none of a predetermined number of memory access requests is to the memory bank; pars. 46-47; Abstract. Examiner further would like to point out that the history register of Nystuen is clearly used for memory requests assignment as in claim 17. Nystuen teaches "history registers 510 and 512 are connected together in series with one another to form a shift register that stores a history of the banks that were accessed with the last two most recent memory access requests; par. 0045."